NEC

MOS FIELD EFFECT TRANSISTOR
2SK3467

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK3467 is N-Channel MOS FET device that features a low on-state resistance and excellent switching characteristics, designed for low voltage high current applications such as DC/DC converter with synchronous rectifier.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3467	TO-220AB(MP-25)
2SK3467-ZK	TO-263(MP-25ZK)

FEATURES

- 4.5-V drive available
- Low on-state resistance
  $R_{DS(on)1}$ = 6.0 mΩ MAX. (V_{GS} = 10 V, I_D = 40 A)
- Low gate charge
  Q_G = 52 nC TYP. (I_D = 80 A, V_{DD} = 16 V, V_{GS} = 10 V)
- Built-in gate protection diode
- Surface mount device available

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	20	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±80	A
Drain Current (Pulse) [Note]	$I_{D(pulse)}$	±240	A
Total Power Dissipation (T_A = 25°C)	P_{T1}	1.5	W
Total Power Dissipation (T_C = 25°C)	P_{T2}	56	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

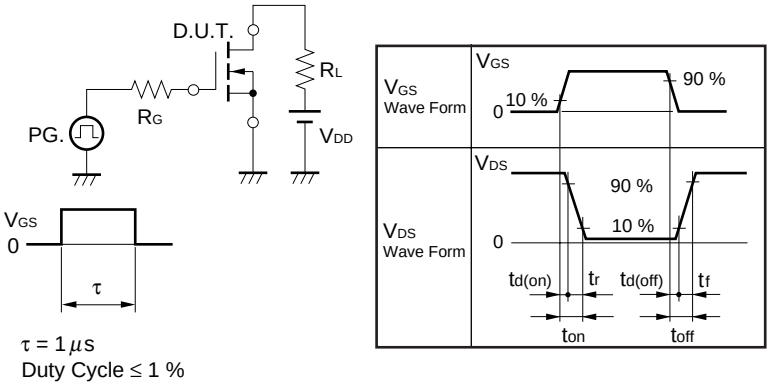
Note PW ≤ 10 μs, Duty Cycle ≤ 1%

Document No. D14991EJ1V0PM00 (1st edition)
Date Published July 2000 NS CP(K)
Printed in Japan

ELECTRICAL CHARACTERISTICS(T_A = 25°C)

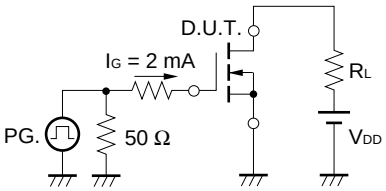
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Leakage Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5		2.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 40 A	14			S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 40 A		4.8	6.0	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 40 A		7.0	10	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		2800		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		1200		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		600		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 10 V , I_D = 40 A		26		ns
Rise Time	t_r	$V_{GS(on)}$ = 10 V		22		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		95		ns
Fall Time	t_f			45		ns
Total Gate Charge	Q_G	V_{DD} = 16 V		52		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		7.2		nC
Gate to Drain Charge	Q_{GD}	I_D = 80 A		18		nC
Diode Forward Voltage	$V_{F(S-D)}$	I_F = 80 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 80 A, V_{GS} = 0 V		50		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		30		nC

TEST CIRCUIT 1 SWITCHING TIME



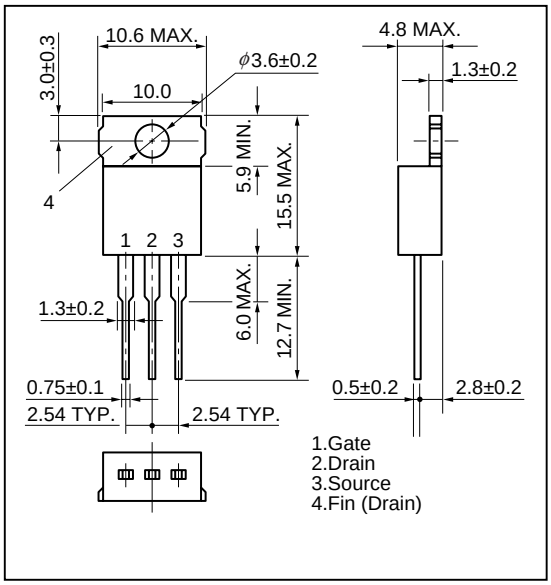
τ = 1 μs
Duty Cycle ≤ 1 %

TEST CIRCUIT 2 GATE CHARGE

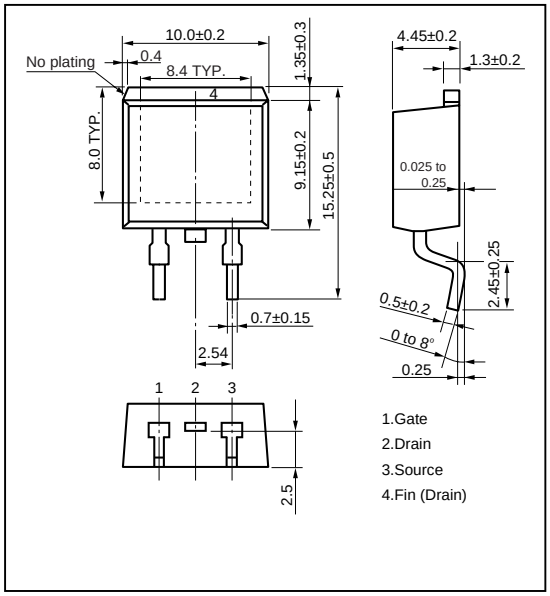


PACKAGE DRAWINGS (Unit : mm)

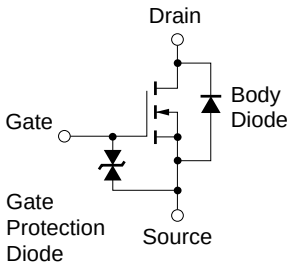
1)TO-220AB (MP-25)



2)TO-263 (MP-25ZK)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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